Notice of Allowability	Application No.	Applicant(s)	
	09/578,440	WASHIO ET AL.	
	Examiner	Art Unit	
	Abbas I Abdulselam	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/21/04*.

2. ☒ The allowed claim(s) is/are *1-31 (renumbered as 1-19, 24-25, 20-21, 26-29, 22-23 and 30-31)*.

3. ☒ The drawings filed on *25 May 2000* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./~~Mail Date~~ 26
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

XIAO WU
PRIMARY EXAMINER

DETAILED ACTION

Allowable Subject Matter

1. The following is an examiner's statement of reasons for allowance:

Moriyama et al (USPN 6232945) teach, a shift register circuit composed of a plurality of cascade-connected flip-flops and responsive to a start pulse, for transferring the start pulse to the succeeding-stage flip-flop in sequence in synchronism with a clock signal; and a reset circuit for outputting a signal for selecting a scanning line on the basis of an output of each-stage flip-flop of the shift register circuit and a reset signal.

Regarding claim 1, none of the cited prior art teaches or suggests a shift register for shifting an input pulse in synchronization with a clock signal, the clock signal being smaller in amplitude than a driving voltage of a control circuit, comprising: flip flops of a plurality of steps that output the input pulse in synchronization with a clock signal, said flip flops being divided into a plurality of blocks, each of the blocks including at least one of said flip flops; and a plurality of level shifters, one of the level shifters corresponding to each of the blocks, wherein each level shifter increases the voltage of the clock signal and applies the clock signal to the corresponding block of flip flops, said shift transmitting the input in synchronization with the clock signal, wherein when one or more of the blocks does not require input of the clock signal, the corresponding level shifter is suspended at that point.

Regarding claim 20 (renumbered as claim 24), none of the cited prior art teaches or suggests a shift register, in which a plurality of flip flops connected, for transmitting an input pulse in synchronization with a clock signal, the clock signal being smaller in amplitude than a driving voltage of a control circuit, comprising: a plurality of level shifters for level-shifting a clock signal, wherein at least one level shifter is provided fro a predetermined number of said flip flops, wherein each level shifter increases the voltage of the clock signal and applies the clock signal to each of the corresponding flip flops, wherein when one or more of the level shifters does not require input of the clock signal, the corresponding level shifter is suspended at that point.

Regarding claim 26 (renumbered as claim 28), none of the cited prior art teaches or suggests a shift register for shifting an input pulse in synchronization with a clock signal, the clock signal being smaller in amplitude than a driving voltage of a control circuit, comprising: flip flops of a plurality of steps that output the input pulse in synchronization with a clock signal, said flip flops being divided into a plurality of blocks, each of the blocks including at least one of said flip flops; and a plurality of level shifters that operate by receiving the input pulse, one of the level shifters corresponding to each of the blocks, wherein each level shifter increases the voltage of the clock signal and applies the clock signal to the corresponding block of flip flops, said shift transmitting the input in synchronization with the clock signal, wherein at least one of said plurality of level shifters corresponding to the block that does not at that point require an input of the clock signal is suspended by a reset in accordance with an output of the level shifter of one of the following blocks.

Regarding claim 27 (renumbered as claim 29), none of the cited prior art teaches or suggests a shift register, in which a plurality of flip flops are connected, for transmitting an input pulse in synchronization with a clock signal by using an output of each flip flops, the output being transmitted to the following flip flop, comprising: a plurality of level shifters for level – shifting the clock signal, the level shifters operating by receiving the input pulse, wherein at least one level shifter is provided for a predetermined number of said flip flops wherein each level shifter increase the voltage of the clock signal and applies the clock signal to each of the corresponding flip flops and each level shifter is rest in accordance with an output of one of the following level shifters.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulselam** whose telephone number is **(703) 305-8591.** The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709.**

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand delivered responses should be brought to Crystal Park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

Abbas Abdulselam

Examiner

Art Unit 2674

December 27, 2004

XIAO WU
PRIMARY EXAMINER